Claims

[c1] 1. A control circuit, comprising:
an output of a first latch connected to an input of a second latch, an output of said second latch connected to an input of a third latch, said second latch having a feedback connection to an input of said first latch and said third latch having feedback connections to said first and said second latches;
combinational logic coupled to said first, second and third latches, said combinational logic having a test signal input, a test clock input and a functional clock input;
said feedback connection of said second latch further coupled through said combinational logic to a first control signal output; and
said first latch coupled through said combinational logic to a second control signal output.

[c2] 2. The circuit of claim 1, wherein:
said second latch is responsive to start a first control signal on said first control signal output after the start of a second control signal based on a first state of a test signal on said test signal input;

said first latch is responsive to start said second control signal on said second control signal output based on said first state of said test signal;
said third latch responsive to terminate said first control signal after a first cycle of a functional clock signal applied to said functional clock input and to terminate said second control signal after a second and consecutive cycle of said functional clock signal after said first cycle of said functional clock signal based on said first state of a test signal on said test signal input; and
said combinational logic responsive to decouple said first control signal from said first control signal output and to couple said test clock input to said second control signal output based on a second state of said test signal.

[c3] 3. The circuit of claim 2, wherein said functional clock signal has a higher frequency than a test clock signal applied to said test clock input.

[c4] 4. The circuit of claim 2, wherein said first and second control signals start and terminate in response to different edges of said functional clock signal.

[c5] 5. The circuit of claim 2, wherein:
said second control signal starts a half a functional clock signal cycle before said first control signal starts; and
said second control signal terminates a half a functional

clock cycle after said first control signal terminates.

[c6] 6. The circuit of claim 2, wherein edges of said first and second control signals are in phase with corresponding edges of said functional clock signal.

[c7] 7. A method of generating control signals, comprising:
connecting an output of a first latch to an input of a second latch;
connecting an output of said second latch to an input of a third latch;
connecting said second latch through a feedback connection to an input of said first latch;
connecting said third latch through feedback connections to said first and said
second latches;
coupling combinational logic to said first, second and third latches, said combinational logic having a test signal input, a test clock input and a functional clock input;
coupling said feedback connection of said second latch through said combinational logic to a first control signal output; and
coupling said first latch through said combinational logic to a second control signal output.

[c8] 8. The method of claim 1, further including:
said second latch starting a first control signal on said

first control signal output after the start of a second control signal in response to a first state of a test signal on said test signal input;
said first latch starting said second control signal on said second control signal output in response to said first state of said test signal;
said third latch terminating said first control signal after a first functional clock signal cycle and terminating said second control signal after a second and consecutive functional clock signal cycle after said first functional clock signal cycle in response to a first state of a test signal on said test signal input; and
said combinational logic decoupling said first control signal from said first control signal output and coupling said test clock input to said second control signal output in response to a second state of said test signal.

[c9] 9. The method of claim 8, wherein said functional clock signal has a higher frequency than a test clock signal applied to said test clock input.

[c10] 10. The method of claim 8, further including:
starting and terminating said first and second control signals in response to different edges of said functional clock signal.

[c11] 11. The method of claim 8, further including:

starting said second control signal at a half functional clock signal cycle of said functional clock signal before starting said first control signal; and
terminating said second control signal at a half functional clock cycle of said functional clock signal after terminating said first control signal.

[c12] 12. The method of claim 7, wherein edges of said first and second control signals are in phase with corresponding edges of said functional clock signal.

[c13] 13. A control circuit, comprising:
an output of a first latch connected to an input of a second latch, an output of said second latch connected to an input of a third latch, said second latch having a feedback connection to an input of said first latch and said third latch having feedback connections to said first and said second latches;
said combinational logic coupled to said first, second and third latches, said combinational logic having a test signal input, a scan enable input and a functional clock input; and
said feedback connection of said second latch further coupled through said combinational logic to a scan control output.

[c14] 14. The circuit of claim 13, wherein:

said first latch is responsive to generate a trigger signal coupled to said second latch based on a first state of a test signal on said test signal input;

said second latch is responsive to said trigger signal to generate a starting edge and a terminating edge of said scan control pulse based on said first state of said test signal;

said third latch is responsive to prevent starting another starting edge of another scan control pulse until said test signal returns to said first state from a second state; and

said combinational logic is responsive to decouple said feedback connection between said second latch and said scan control output and to couple said scan enable input to said scan control output based on a second state of said test signal.

[c15] 15. The circuit of claim 14, wherein said functional clock signal has a higher frequency than a scan control signal on said scan control input.

[c16] 16. The circuit of claim 14, wherein said starting and terminating edges of said scan control pulse are generated in response to edges of said functional clock signal.

[c17] 17. The circuit of claim 14, wherein scan control pulse has a duration of a single cycle of said functional clock

cycle in duration.

[c18] 18. The circuit of claim 14, wherein said starting and terminating edges said scan control pulse are in phase with corresponding edges of said functional clock signal.

[c19] 19. A method of generating a control signal, comprising:
connecting an output of a first latch to an input of a second latch;
connecting an output of said second latch to an input of a third latch;
connecting said second latch through a feedback connection to an input of said first latch;
connecting said third latch through feedback connections to said first and said second latches;
coupling combinational logic to said first, second and third latches, said combinational logic having a test signal input, a scan enable input and a functional clock input; and
coupling said feedback connection of said second latch through said combinational logic to a scan control output.

[c20] 20. The method of claim 19, further including:
said first latch generating a trigger signal coupled to said second latch in response to a first state of a test signal on said test signal input;

said second latch, in responsive to said trigger signal, generating a starting edge and a terminating edge of said scan control pulse based on said first state of said test signal;

said third latch preventing starting another starting edge of another scan control pulse until said test signal returns to said first state from a second state; and

said combinational logic decoupling said feedback connection from said second latch from said scan control output and coupling said scan enable input to said scan control output in response to a second state of said test signal.

[c21] 21. The method of claim 20, wherein said functional clock signal has a higher frequency than a scan control signal on said scan control input.

[c22] 22. The circuit of claim 20, further including:
generating said starting and terminating edges of said scan control pulse in response to edges of said functional clock signal.

[c23] 23. The circuit of claim 20, wherein scan control pulse has a duration of a single cycle of said functional clock cycle in duration.

[c24] 24. The circuit of claim 20, wherein said starting and

terminating edges of said scan control pulse are in phase with corresponding edges of said functional clock signal..

[c25] 25. An integrated circuit, comprising:
a test pin, a first test clock pin, a second test clock pin, a third test clock pin a functional clock pin, a scan-in pin, a scan-out pin and an enable pin;
a test controller having a test input connected to said test pin, a first test clock input connected to said first test clock pin, a functional clock input connected to said functional clock pin, a first control output and a second control output;
a clock splitter having a first clock input connected to said second test clock pin, a second clock input connected to said functional clock pin, a first control input connected to said first control output of said test controller, a second control input connected to said second control output and of said controller, an enable input connected to said enable pin, a ZB clock output and a ZC clock output; and
an LSSD scan chain comprised of serially connected latches, a first stage of each latch having an first data input, a second data input and a C clock input connected to said ZC clock output of said clock splitter, an A CLK input connected to said third test clock pin, a second

stage of each latch having a data output and a B clock input connected to said ZB clock output of said clock splitter, a data output of a previous latch connected to a first input pin of an immediately subsequent latch, a first data input of a first latch of said LSSD scan chain connected to said scan-in pin and a data output pin of a last scan chain latch of said scan chain connected to said scan-out pin.

[c26] 26. The circuit of claim 25, wherein said test controller includes:

an output of a first latch connected to an input of a second latch, an output of said second latch connected to an input of a third latch, said second latch having a feedback connection to an input of said first latch and said third latch having feedback connections to said first and said second latches;

combinational logic coupled to said first, second and third latches, said combinational logic coupled to said test pin, said first test clock pin and said functional clock pin;

said first latch coupled through said combinational logic to said second control output; and

said feedback connection of said second latch further coupled through said combinational logic to said first control output.

[c27] 27. The circuit of claim 25, further including:
additional clock splitters connected to said test controller, some or all of said additional clock splitters connected to corresponding additional scan chains.

[c28] 28. The circuit of claim 25, wherein:
said test controller is responsive to generate a first control signal having a duration of one cycle of said functional clock signal on said first control pin and to generate a second control signal having a duration of two cycles of said functional clock signal on said second control output upon a transition from a first state to a second state of a test signal applied to said test pin, said first control signal starting a half cycle of said functional clock cycle after the start of said second control signal; and
said clock splitter is responsive to generate a first B clock pulse, followed by a C clock pulse, followed by a second B clock pulse, said B and C clock pulses at the same frequency as said functional clock signal, based on said first and second control signals.

[c29] 29. The circuit of claim 28, wherein:
(a) if said functional clock is in a high state prior to said test signal transitioning to a high state then, within a sequence of five consecutive edges of said functional clock

signal each edge defining a change of state of said functional clock signal, said second control signal is generated on a first edge and terminated on a fifth edge and said first control signal is generated on a second edge and terminated on a fourth edge of said sequence of five consecutive edges of said functional clock signal; and
(b) if said functional clock is in a low state prior to said test signal transitioning to a high state, then within a sequence of four consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, said second control signal is generated on a first edge and terminated on a fourth edge and said first control signal is generated on a first edge and terminated on a third edge of said sequence of four consecutive edges of said functional clock signal.

[c30] 30. The circuit of claim 28, wherein:
(a) if said functional clock is in a high state prior to said test signal transitioning to a high state, then within a given sequence of five consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, said first B clock pulse is generated on a second edge and terminated on a third edge, said C clock pulse is generated on said third edge and terminated on a fourth edge, and said second B clock pulse is generated on said fourth edge and termi-

nated on a fifth edge of said sequence of five consecutive edges of said functional clock signal; and

(b) if said functional clock is in a low state prior to said test signal transitioning to a high state, then within a given sequence of four consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, said first B clock pulse is generated on a first edge and terminated on a second edge, said C clock pulse is generated on said second edge and terminated on a third edge, and said second B clock pulse is generated on said third edge and terminated on a fourth edge of said sequence of five consecutive edges of said functional clock signal.

[c31] 31. The circuit of claim 28, wherein said first and second B clock pulses cause data in said first stages of said latches to be captured by said second stages of said latches and said C clock pulse causes data states on said data pin to be latched by said first stages of said latches.

[c32] 32. The circuit of claim 28, wherein:

said functional clock signal has a higher frequency than that of a B test clock signal applied to said first test clock pin and that of a C test clock signal applied to said second test clock pin; and

when said test signal is in said second state, data previously entered into first stages of said latches while said B

test clock signal was applied to said first test clock pin and while said C clock test signal was applied to second test clock pin is prevented from being replaced until after a data transfer from said first stages of said latches to second stages of said latches while said functional clock signal is applied to said first and second test clock pins instead of said B test clock and C test clock signals.

[c33] 33. The circuit of claim 28, wherein said test controller is further adapted to generate no more than one pulse of said first control signal and one pulse of said second control signal without a transition of said test signal from said first state to a second state intervening.

[c34] 34. A method of testing an integrated circuit, comprising:

providing a test pin, a first test clock pin, a second test clock pin, a third clock pin, a functional clock pin, a scan-in pin, a scan-out pin and an enable pin;

providing a test controller having a test input connected to said test pin, a first test clock input connected to said first test clock pin, a functional clock input connected to said functional clock pin, a first control output and a second control output;

providing a clock splitter having a first clock input connected to said second test clock pin, a second clock input connected to said functional clock pin, a first control

input connected to said first control output of said test controller, a second control input connected to said second control output and of said controller, an enable input connected to said enable pin, a ZB clock output and a ZC clock output; and

providing an LSSD scan chain comprised of serially connected latches, a first stage of each latch having a first data input, a second data input and a C clock input connected to said ZC clock output of said clock splitter, an A clock input connected to said third test clock pin, a second stage of each latch having a data output and a B clock input connected to said ZB clock output of said clock splitter, a data output of a previous latch connected to a first input pin of an immediately subsequent latch, a first data input of a first latch of said LSSD scan chain connected to said scan-in pin and a data output pin of a last scan chain latch of said scan chain connected to said scan-out pin.

[c35] 35. The method of claim 34, wherein said test controller includes:

an output of a first latch connected to an input of a second latch, an output of said second latch connected to an input of a third latch, said second latch having a feedback connection to an input of said first latch and said third latch having feedback connections to said first

and said second latches;
combinational logic coupled to said first, second and third latches, said combinational logic coupled to said test pin, said first test clock pin and said functional clock pin;
said first latch coupled through said combinational logic to said second control output; and
said feedback connection of said second latch further coupled through said combinational logic to said first control output.

[c36] 36. The method of claim 34, further including:
connecting additional clock splitters to said test controller, some or all of said additional clock splitters connected to corresponding additional scan chains.

[c37] 37. The method of claim 34, further including:
said test controller generating a first control signal of one cycle of said functional clock signal in duration on said first control pin and generating a second control signal having a duration of two cycles of said functional clock signal on said second control output upon a transition from a first state to a second state of a test signal applied to said test pin, said first control signal starting at half cycle of said functional clock cycle after the start of said second control signal; and
said clock splitter generating a first B clock pulse, fol-

lowed by a C clock pulse, followed by a second B clock pulse, said B and C clock pulses at the same frequency as said functional clock signal, based on said first and second control signals..

[c38] 38. The method of claim 37, further including:
(a) if said functional clock is in a high state prior to said test signal transitioning to a high state then, within a sequence of five consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, generating said second control signal on a first edge, terminating said second control signal on a fifth edge, generating said first control signal on a second edge and terminating said first control signal on a fourth edge of said sequence of five consecutive edges of said functional clock signal; and
(b) if said functional clock is in a low state prior to said test signal transitioning to a high state, then within a sequence of four consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, generating said second control signal on a first edge, terminating said second control signal on a fourth edge, generating said first control signal on a first edge and terminating said first control signal on a third edge of said sequence of four consecutive edges of said functional clock signal.

[c39] 39. The method of claim 37, further including:

(a) if said functional clock is in a high state prior to said test signal transitioning to a high state, then within a given sequence of five consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, generating said first B clock pulse on a second edge and terminating said first B clock pulse on a third edge, generating said C clock pulse on said third edge and terminating said C clock pulse on a fourth edge, and generating said second B clock pulse on said fourth edge and terminating said second B clock pulse on a fifth edge of said sequence of five consecutive edges of said functional clock signal; and

(b) if said functional clock is in a low state prior to said test signal transitioning to a high state, then within a given sequence of four consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, generating said first B clock pulse on a first edge, and terminating said first B clock pulse on a second edge, generating said C clock pulse on said second edge and terminating said C clock pulse on a third edge, and generating said second B clock pulse on said third edge and terminating said second B clock pulse on a fourth edge of said sequence of

five consecutive edges of said functional clock signal.

[c40] 40. The method of claim 37, further including:
capturing data said second stages of said latches in response to said first and second B clock pulses; and
latching data states on said data pins of said first stages of said latches in response to said C clock pulse.

[c41] 41. The method of claim 37, wherein:
said functional clock signal has a higher frequency than that of a B test clock signal applied to said first test clock pin and that of a C test clock signal applied to said second test clock pin; and
when said test signal is in said second state, data previously entered into first stages of said latches while said B test clock signal was applied to said first test clock pin and while said C clock test signal was applied to second test clock pin is prevented from being replaced until after a data transfer from said first stages of said latches to second stages of said latches while said functional clock signal is applied to said first and second test clock pins instead of said B test clock and C test clock signals.

[c42] 42. The method of claim 37, further including said test controller generating no more than one pulse of said first control signal and one pulse of said second control signal without a transition of said test signal from said

first state to a second state intervening.

[c43] 43. An integrated circuit, comprising:
a test pin, a select enable pin, a functional clock pin, a scan-in pin and a scan-out pin;
a test controller having a test input connected to said test pin, a functional clock input connected to said functional clock pin, a first control output and a second control output;
a scan chain comprised of serially connected latches and corresponding multiplexers, a first stage of each latch having a data input, a clock input connected to a functional clock pin, a first control input connected to said first control output of said test controller, a second stage of each latch having a data output and a second control input connected to said second control output of said tester controller, a data output of a previous latch connected to a first selectable input of a multiplexer corresponding to an immediately subsequent latch, a selected output of said corresponding multiplexer connected to said data input of said immediately subsequent latch, a first selectable data input of a multiplexer of said scan chain connected to said scan-in pin and a data output of a last latch of said scan chain connected to said scan-out pin.

[c44] 44. The circuit of claim 43, wherein said test controller includes:
an output of a first latch connected to an input of a second latch, an output of said second latch connected to an input of a third latch, said second latch having a feedback connection to an input of said first latch and said third latch having feedback connections to said first and said second latches;
combinational logic coupled to said first, second and third latches, said combinational logic coupled to said test pin, said functional clock pin;
said first latch coupled through said combinational logic to said first control output; and
said feedback connection of said second latch further coupled through said combinational logic to said second control output.

[c45] 45. The circuit of claim 43, wherein:
said test controller is responsive to generate a first control signal of one cycle of said functional clock signal in duration on said first control pin upon a transition from a first state to a second state of a test signal applied to said test pin;
said test controller is responsive to generate a second control signal on said second control output upon said transition from said first state to said second state of

said test signal applied to said test pin; and
said second control signal having a duration of two cycles of a functional clock signal applied to said functional clock pin and said first control signal starting at a half cycle of said functional clock cycle after the start of said second control signal.

[c46] 46. The circuit of claim 45, wherein:
(a) if said functional clock is in a high state prior to said test signal transitioning to a high state then, within a sequence of five consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, said second control signal is generated on a first edge and terminated on a fifth edge, and said first control signal is generated on a second edge and terminated on a fourth edge of said sequence of five consecutive edges of said functional clock signal; and
(b) if said functional clock is in a low state prior to said test signal transitioning to a high state, then within a sequence of four consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, said second control signal is generated on a first edge and terminated on a fourth edge, and said first control signal is generated on a first edge and terminated on a third edge of said sequence of four consecutive edges of said functional clock signal.

[c47] 47. The circuit of claim 45, wherein said first control signal causes data on said selected outputs of said multiplexers of said scan chains to be latched by said first stages of said latches and said second control signal causes data in said first stages of said latches to be captured by said second stages of said latches.

[c48] 48. The circuit of claim 45, wherein:
when said test signal is in said second state, data previously entered into first stages of said latches while said test signal was in said first state is prevented from being replaced until after a data transfer from said first stages of said latches to second stages of said latches while said test signal is in said second state.

[c49] 49. The circuit of claim 43, wherein each latch of said scan chain includes a clock gate control circuit coupled between said first and second control inputs of said latches and said clock input.

[c50] 50. The circuit of claim 49, wherein said clock gate control circuit is responsive to said first and second control to prevent further signal propagation between said output of said clock selection circuit and said clock input pins of said latches after termination of said control signal.

[c51] 51. A method of testing an integrated circuit, comprising:

providing a test pin, a select enable pin, a functional clock pin, a scan-in pin and a scan-out pin;

providing a test controller having a test input connected to said test pin, a functional clock input connected to said functional clock pin, a first control output and a second control output;

providing a scan chain comprised of serially connected latches and corresponding multiplexers, a first stage of each latch having a data input, a clock input connected to a functional clock pin, a first control input connected to said first control output of said test controller, a second stage of each latch having a data output and a second control input connected to said second control output of said tester controller, a data output of a previous latch connected to a first selectable input of a multiplexer corresponding to an immediately subsequent latch, a selected output of said corresponding multiplexer connected to said data input of said immediately subsequent latch, a first selectable data input of a multiplexer of said scan chain connected to said scan-in pin and a data output of a last latch of said scan chain connected to said scan-out pin.

[c52] 52. The circuit of claim 51, wherein said test controller includes:
an output of a first latch connected to an input of a second latch, an output of said second latch connected to an input of a third latch, said second latch having a feedback connection to an input of said first latch and said third latch having feedback connections to said first and said second latches;
combinational logic coupled to said first, second and third latches, said combinational logic coupled to said test pin, said first test clock pin and said functional clock pin;
said first latch coupled through said combinational logic to said second control output; and
said feedback connection of said second latch further coupled through said combinational logic to said first control output.

[c53] 53. The method of claim 51, further including:
said test controller generating a first control signal having a duration of one cycle of said functional clock signal on said first control pin upon a transition from a first state to a second state of a test signal applied to said test pin;
said test controller generating a second control signal on said second control output upon said transition from

said first state to said second state of said test signal applied to said test pin; and
said second control signal having a duration of two cycles of a functional clock signal applied to said functional clock pin and said first control signal starting at a half cycle of said functional clock cycle after the start of said second control signal.

[c54] 54. The method of claim 53, further including:
(a) if said functional clock is in a high state prior to said test signal transitioning to a high state then, within a sequence of five consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, generating said second control signal on a first edge and terminating said second control signal on a fifth edge, and generating said first control signal on a second edge and terminating said first control signal on a fourth edge of said sequence of five consecutive edges of said functional clock signal; and
(b) if said functional clock is in a low state prior to said test signal transitioning to a high state, then within a sequence of four consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, generating said second control signal on a first edge and terminating said second control signal on a fourth edge, and generating said first

control signal on a first edge and terminating said first control signal on a third edge of said sequence of four consecutive edges of said functional clock signal.

[c55] 55. The method of claim 53, further including:
latching data on said selected outputs of said multiplexers of said scan chains by said first stages of said latches in response to said first control signal and capturing data in said first stages of said latches by said second stages of said latches in response to said second control signal.

[c56] 56. The method of claim 53, wherein:
when said test signal is in said second state, data previously entered into first stages of said latches while said test signal was in said first state is prevented from being replaced until after a data transfer from said first stages of said latches to the second stages of said latches while said test signal is in said second state.

[c57] 57. The method of claim 53, further including:
coupling a clock gate control circuit between said first and second control inputs of said latches and said clock input.

[c58] 58. The method of claim 57, wherein said clock gate control circuit is responsive to said first and second con-

trol signals generated on said first and second control outputs of said test controller in order to prevent signal propagation between said output of said clock selection circuit and said clock input pins of said latches after termination of said control signal.

[c59] 59. An integrated circuit, comprising:
a test pin, a select enable pin, a functional clock pin, a scan-in pin and a scan-out pin;
a test controller having a test input connected to said test pin, a select enable input connected to said select enable pin, a functional clock input connected to said functional clock pin, and a control output;
a scan chain comprised of serially connected latches and corresponding de-multiplexers, a first stage of each latch having a data input and a clock input connected to a functional clock pin, a second stage of each latch having a data output, a data output of a previous latch connected to a first selectable input of a multiplexer corresponding to an immediately subsequent latch, a selected output of said corresponding multiplexer connected to said data input of said immediately subsequent latch, a first selectable data input of a multiplexer of said scan chain connected to said scan-in pin and a selected output of a last latch of said scan chain connected to said scan-out pin and each multiplexer of said scan chain

having a select input connected to said control output of said test controller.

[c60] 60. The circuit of claim 59, wherein said test controller includes:
an output of a first latch connected to an input of a second latch, an output of said second latch connected to an input of a third latch, said second latch having a feedback connection to an input of said first latch and said third latch having feedback connections to said first and said second latches;
said combinational logic coupled to said first, second and third latches, said test input, said select enable input and said functional clock input; and
said feedback connection of said second latch further coupled through said combinational logic to said control output.

[c61] 61. The circuit of claim 59, wherein a control pulse generated by said test controller on said control output has a duration of one cycle of a functional clock signal applied to said functional clock pin.

[c62] 62. The circuit of claim 61, wherein said control pulse enables data on data pins of said multiplexers of said scan chains to be latched by said first stages of said latches on a first functional clock pulse and scan data

out of said scan chain on subsequent pulses of said functional clock signal.

[c63] 63. The circuit of claim 61, wherein:
(a) if a functional clock signal on said functional clock pin is in a low state prior to a test signal on said test pin transitioning from a first to a second state then, within a sequence of four consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, said control pulse is generated on a first edge and terminated on a fourth edge of said sequence of four consecutive edges of said functional clock signal; and
(b) if said functional clock signal is in a low state prior to said test signal transitioning from said first state to said second state, then within a sequence of five consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, said control pulse is generated on a second edge and terminated on a fifth edge of said sequence of five consecutive edges of said functional clock signal.

[c64] 64. The circuit of claim 59, wherein:
when said test signal is in said second state, data previously entered into first stages of said latches while said test signal was in said first state is prevented from being replaced until after a data transfer from said first stages

of said latches to second stages of said latches while said test signal is in said second state.

[c65] 65. A method of testing an integrated circuit, comprising:
providing a test pin, a select enable pin, a functional clock pin, a scan-in pin and a scan-out pin;
providing a test controller having a test input connected to said test pin, a select enable input connected to said select enable pin, a functional clock input connected to said functional clock pin, and a control output;
providing a scan chain comprised of serially connected latches and corresponding multiplexers, a first stage of each latch having a data input and a clock input connected to a functional clock pin, a second stage of each latch having a data output, a data output of a previous latch connected to a first selectable input of a multiplexer corresponding to an immediately subsequent latch, a selected output of said corresponding multiplexer connected to said data input of said immediately subsequent latch, a first selectable data input of a multiplexer of said scan chain connected to said scan-in pin and a selected output of a last latch of said scan chain connected to said scan-out pin and each multiplexer of said scan chain having a select input connected to said control output of said test controller.

[c66] 66. The method of claim 65, wherein said test controller includes:
an output of a first latch connected to an input of a second latch, an output of said second latch connected to an input of a third latch, said second latch having a feedback connection to an input of said first latch and said third latch having feedback connections to said first and said second latches;
said combinational logic coupled to said first, second and third latches, said test input, said select enable input and said functional clock input; and
said feedback connection of said second latch further coupled through said combinational logic to said control output.

[c67] 67. The method of claim 65, wherein a control pulse generated on by said test controller on said control output has a duration of one cycle of a functional clock signal applied to said functional clock pin.

[c68] 68. The method of claim 67, further including:
(a) if a functional clock signal on said functional clock pin is in a low state prior to a test signal on said test pin transitioning from a first to a second state then, within a sequence of four consecutive edges of said functional clock signal each edge defining a change of state of said

functional clock signal, generating said control pulse on a first edge and terminating said control pulse on a fourth edge of said sequence of four consecutive edges of said functional clock signal; and

(b) if said functional clock signal is in a low state prior to said test signal transitioning from said first state to said second state, then within a sequence of five consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, generating said control pulse on a second edge and terminating said control pulse on a fifth edge of said sequence of five consecutive edges of said functional clock signal.

[c69] 69. The method of claim 67, further including said control pulse enabling data on data pins of said multiplexers of said scan chains to be latched by said first stages of said latches on a first functional clock pulse and enabling data to be scanned out of said scan chains on subsequent pulses of said test clock signal.

[c70] 70. The method of claim 69, wherein:

when said test signal is in said second state, data previously entered into first stages of said latches while said test signal was in said first state is prevented from being replaced until after a data transfer from said first stages of said latches to second stages of said latches while said test signal is in said second state.